spectracom

TSync-PCI-104

PCI-104 TIME CODE PROCESSOR
with optional GNSS RECEIVER

User Manual



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www.spectracomcorp.com

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Returned products must be returned with a description of the claimed defect, the RMA number, and the name and contact information of the individual to be contacted if additional information is required by Spectracom. Products being returned on an RMA must be properly packaged with transportation charges prepaid.

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CHAPTER 1

Safety and Compliance

This chapter contains information that is relevant not only for your per sonal safety, but can also help prevent potential damage when working with the equipment. Also included in this chapter is information about legal compliance, and pertinent technical standards to which this product adheres.



Figure 1-1: Do not ignore the Safety Instructions

This chapter discusses the following:

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1.1 Safety Symbols

The following symbols are used in Spectracom technical documentation.

Symbol	Signal word	Definition
	DANGER!	Potentially dangerous situation which may lead to personal injury or death! Follow the instructions closely.
	CAUTION!	Potential equipment damage or destruction! Follow the instructions closely.
	NOTE	Tips and other useful or important information.
	ESD	Risk of ElectroStatic Discharge! Avoid potential equipment damage by following ESD Best Practices.
	CHASSIS GROUND	Never remove or loosen cables or screws serving as chassis ground to prevent potentially dangerous situations.
	Analog Ground	Do not tamper with Analog Ground, in order to prevent impaired functionality of the equipment.
	Recycle	Recycle the mentioned components at their end of life. Follow local laws.

Table 1-1: Spectracom safety symbols

1.2 About Safety

This product has been designed and built in accordance with state-of-the-art standards and the recognized safety rules. Nevertheless, its use may constitute a risk to the operator or installation/maintenance personnel, if used under conditions that must be deemed unsafe, or for purposes other than the product's designated use, which is described in the introductory technical chapters of this guide.

1.2.1 Basic Responsibilities

- The equipment must only be used in technically perfect condition. Check components for damage prior to installation. Also check for loose or scorched cables on other nearby equipment.
- Make sure you possess the professional skills, and have received the train ing necessary for the type of work you are about to perform (for example *Best Practices in ESD prevention*.)
- Do not modify the equipment, and use only spare parts authorized by Spec tracom.
- Always follow the instructions set out in this guide.
- Observe generally applicable legal and other local mandatory regulations.

1.2.2 Other Safety Tips

Keep these instructions at hand, near the place of use. Keep your workplace tidy. Apply technical common sense: If you suspect that it is unsafe to use the product, do the following:

- Disconnect the supply voltage from the (main) unit, e.g. by unplug ging the line cord.
- Clearly mark the equipment to prevent its further operation.

1.3 Compliance

This equipment has been tested and found to comply with the following standards:

Safety:

EN-60950-1:2006/A1:2010 Safety of Information Technology Equipment

EMC:

CISPR 11 (2003): Radiated and Conducted Emissions
EN-61236-1: 2006 Consisting of:

- EN61000-3-2 (2000): Harmonic Current Emissions
- EN61000-3-3 (2002): Voltage Fluctuations and Flicker in Low Voltage
- EN61000-4-2 (2001): Electrostatic Discharge Immunity
- EN61000-4-3 (2002): Radiated Electric Field Immunity

- EN61000-4-4 (2004): Electric Fast Transit Burst Immunity
- EN61000-4-5 (2001): High Voltage Surge Immunity
- EN61000-4-6 (2003): RF Common Mode Immunity
- EN61000-4-11 (2004): Voltage Dip and Interrupt Immunity

Supplementary Information

This product complies with the requirements of the **Low Voltage Directive 2006/95/EC** and the **EMC Directive 2004/108/EC**, and with the European Union Directive **2002/95/EC** on the Restriction of Hazardous Substances in Elec trical and Electronic Equipment (RoHS).

EN-electro-magnetic compliance

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful inter ference in which case the user will be required to correct the interference at his/her own expense.

Underwriters Laboratory (UL)

Underwriters Laboratory (UL) has not tested the performance or reliability of the Global Positioning System (GPS) hardware, operating software, or other aspects of this product. UL has only tested for fire, shock, or casualties as outlined in UL's Stand ard(s) for Safety for Information Technology Equipment, UL60950-1. UL Cer tification does not cover the performance or reliability of the GPS hardware and GPS operating software.

UL MAKES NO REPRESENTATIONS, WARRANTIES, OR CERTIFICATIONS WHATSOEVER REGARDING THE PERFORMANCE OR RELIABILITY OF ANY GPS RELATED FUNCTIONS OF THIS PRODUCT.

CHAPTER 2

Overview

In this chapter, you will find information about fundamental technical concepts pertaining to the TSync-PCI-104 card, as well as setup and installation.

This chapter discusses the following:

2.1 General Information about GPS and GNSS 6
2.2 Your Spectracom GNSS Receiver 7
2.3 Inventory 7
2.4 Inspection and Support 7

The TSync-PCI-104 with optional internal GNSS receiver is a complete synchronized timecode reader/generator package that supports multiple prioritized timing inputs. When an input is lost, the unit automatically switches to the next input in order of priority.

The disciplined onboard oscillator is phase-locked to an external timing input, providing 5ns resolution time. This 10-MHz oscillator, central to the TSync-PCI-104 timing functions, uses the last known reference to increment ("freewheel") in the absence of a timing input.

The TSync-PCI-104 generates an IRIG AM and DCLS output pair, as well as 10 MHz sine wave and 1PPS outputs.

The board's four programmable inputs may be used as event capture inputs, dedicated to your time-tagging applications. Four user-programmable alarm and frequency outputs are also provided. Programmable output functions include a periodic pulse or "heartbeat," square wave, and programmable start/stop time "alarm" output.

Key to the TSync-PCI-104's functionality is the ability to generate interrupts. Using one of the many available Spectracom driver packages, you may configure your card using interrupt-driven algorithms to support your unique applications.

2.1 General Information about GPS and GNSS

The United States government operates a set of approximately 32 satellites, collectively known as the "GPS constellation" or "GPS satellites." Each satellite has an internal atomic clock and transmits a signal specifying the time and satellite position. On the ground, the GPS receiver determines its position (longitude, latitude and elevation) and the time by decoding the signals simultaneously from at least four of the GPS satellites. Each satellite transmits a signal in the L1 band at a frequency of 1575.42 MHz. When power is first applied, the GPS receiver begins searching for the satellites. This process can take a few minutes, as the receiver iteratively locates satellites, refines its position, and determines for which satellites to search.

The GPS receiver retains the last known position when the power is switched off. This results in faster satellite acquisition the next time it is switched on. If the antenna has been moved more than a few miles, however, acquisition time will be slightly longer because it must first recompute the position.

This unit is capable of using other Global Navigation Satellite Systems (GNSS) alongside, or instead of, GPS: The Russian GLONASS system is fully operational with 24 satellites each transmitting at a frequency between 1598 and 1606 MHz. This GPS/GLONASS frequency diversity offers improved performance in some environments when using dual-mode GPS+GLONASS receivers. Other benefits are

system redundancy and the availability of additional satellites when using GPS and GLONASS together.

2.2 Your Spectracom GNSS Receiver

This TSync-PCI-104 system is available with an internal GNSS receiver, which is mounted to the unit.

The board supplies 5 VDC through the receiver module to the external antenna via the coaxial cable.



NOTE – The GNSS receiver and the Spectracom GNSS antenna are compatible with GLONASS. Utilizing this functionality does not require any additional setup by the user.

2.3 Inventory

Before installing the board, please verify that all material ordered has been received:

All boards are shipped with a break-out cable and a user manual.

Also included is an SMA-to-Type-N-RF-adapter-cable.

Should there be any discrepancy between items ordered and items shipped and received, please contact Spectracom Customer Service at US +1.585.321.5800.

2.4 Inspection and Support

Unpack the equipment and inspect it for damage. If any equipment has been dam aged in transit, please contact Spectracom Customer Service at US +1.585.321.5800.

If any problems occur during installation and configuration of your Spectracom product, please contact Spectracom Technical Support at US 585.321.5823 or US 585.321.5824.

Electronic equipment is sensitive to Electrostatic Discharge (ESD). Observe all ESD precautions and safeguards when handling the timecode generator.

NOTE – If equipment is returned to Spectracom, it must be shipped in its original packing material. Save all packaging material for this purpose.

CHAPTER 3

Specifications

This chapter discusses the following:

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3.1 General Specifications

- Bus Interface: Universal Signaling Voltage 3.3 V/5 V
- Bus speed: 32-bit address @ 33/66 MHz
- Compliant with PCI Local Bus Specification Revision 2.2
- PCI-104 Specification Ver. 1.1

3.1.1 Dimensions

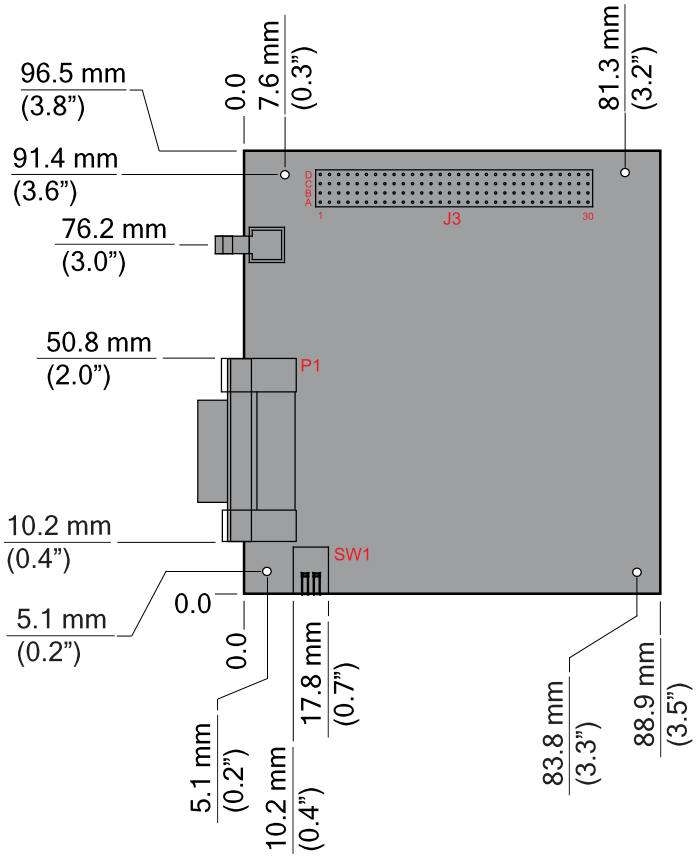


Figure 3-1: Board layout and dimensions

3.2 PCI-104 Power

- +5 VDC ±5% @ 1.4 A typical
- +3.3 V ±5%, 0.7 A typical
- +12 V ±8%, 0.2 A typical
- -12 VDC ±5% @ 0.2 A typical

3.3 IRIG AM Input

- IRIG AM input at timing interface connector
- Accepts IRIG Formats A, B, G; NASA36; IEEE 1344
- Amplitude: 500 mV_{p-p} to 10 V_{p-p}
- Modulation ratio: 2:1 minimum, 6:1 maximum
- Input impedance: 10k-ohm minimum
- DC Common Mode Voltage: ±150 VDC maximum
- Input Stability: Better than 100 ppm

3.4 IRIG DCLS Input

- IRIG DCLS Input at timing interface connector
- Accepts IRIG formats A, B, G; NASA36; IEEE 1344 pulse width codes (does not accept Manchester modulated codes)
- RS-485 differential input: -7 V to +12 V common mode voltage input range, 200 mVp-p differential voltage threshold
- Single-ended input:
  - +1.3 $V_{VIL\ min}$, +2 $V_{VIH\ max}$
  - +1.45 $V_{VIL\ typ}$, +1.85 $V_{VIH\ typ}$

3.5 IRIG AM Output

- IRIG AM output at timing interface connector
- Outputs formats A, B, E (100 Hz, 1 KHz), G; NASA36; IEEE 1344

- Amplitude:
  - 0.5 V_{p-p} to 6 V_{p-p} into 50 ohms, user settable
  - 1 V_{p-p} to 12 V_{p-p} into > 600 ohms
- Output impedance: 50 ohm nominal
- Output load: 50 ohm minimum
- Modulation ratio: 3:1 nominal
- Accuracy: ±2 to 200 microseconds (IRIG-format dependent)

3.6 IRIG DCLS Output

- IRIG DCLS output at timing interface connector
- Outputs formats A, B, E, G; NASA36; IEEE 1344 pulse width codes (does not generate Manchester modulated codes)
- RS-485 differential signal:
  - 1.8 V_{max} common mode output voltage (RS-485 compatible)
  - 1.5 V_{min} to 3.3 V max differential output voltage swing
- Single-ended amplitude (100 Ohm load):
  - 0.5 V V_{OL} max, +2.5 V V_{OH} min (TTL compatible)

3.7 10-MHz Output

- 10-MHz sine wave output from oscillator
- Output impedance: 50 ohm nominal
- Output load: 50 ohm minimum
- Output harmonics: < -40 dBc
- Output spurious: < -70 dBc

	TCXO	OCXO
Accuracy (average over 24 hours when GNSS locked)	$1x10^{-11}$	$5x10^{-12}$
Medium term stability (without CPS after 2 weeks of GNSS lock)	$1x10^{-8}$/day	$2x10^{-9}$/day
Phase noise (dBc/Hz)		

	TCXO	OCXO
@1 Hz	—	-85
@10 Hz	—	-113
@100 Hz	-110	-120
@1 KHz	-135	-140
@10 KHz	-140	-150
Signal wave form & levels: +13 dBm into 50 ohm, ±3 dB		

Table 3-1: 10-MHz output specifications

3.8 External 1PPS Input

- External 1PPS reference input to timing connector
- 1 Hz pulse, *rising edge* or *falling edge active* (selectable)
  - 100 nsec. minimum pulse width
- 0 V to + 5.5 V input range, +0.8 V_{VIL}, +2.0 V_{VIH}
- Input impedance <150 pF capacitive

3.9 1PPS Output

- 1PPS output at timing interface connector
- 1Hz pulse, *rising edge* or *falling edge active* (selectable)
  - 40 ns to 900 ms active pulse width (selectable, 200 ms default)
- Rise time: <10 ns
- Signal level: TTL compatible, 4.3 V_{min}, base-to-peak into 50 ohms
- Accuracy:
  - Positive edge within ±50 nanoseconds of UTC when locked to a valid 1PPS input reference

	TCXO	OCXO
Accuracy to UTC (1-sigma locked to GPS)	±50 ns	±50 ns
Holdover (constant temp after 2 weeks of GNSS lock)		
After 4 hours	12 µs	3 µs
After 24 hours	450 µs	100 µs

3.10 GPIO Inputs

- GPIO inputs to timing connector
- 50 ns active pulse width minimum
- 50 ns minimum between pulses
- 0V to +5.5 V input range, +0.8 V_{VIL}, +2.0 V_{VIH}
- Input impedance <150 pF capacitive

3.11 GPIO Outputs

- GPIO outputs from timing connector
- Pulse output: 20 ns to 900 ms active pulse width
- Square wave output:
  - 100 ns to 20 second period
  - 20 ns to 900 ms Active Pulse Width
- Amplitude: TTL compatible, 4.3 V_{min}, base-to-peak into 50 ohms

3.12 On-Board GPS RF Connector (Internal GNSS Receiver)

The on-board GNSS RF connector supports the RF connection between the on-board GNSS receiver and an external L1 antenna. It consists of a female SMA connector. A short male SMA to female N cable made from RG-316 coax is provided to con nect to the antenna RF cable.

NOTE – The provided cable should be used instead of an adapter. This relieves strain on the connectors.

3.12.1 Electrical Characteristics, GNSS RF Signal

- L1 GPS/GLONASS signals from antenna to on-board GPS receiver
- 30 mA @ +5 V (±10%) provided to power antenna

3.13 GNSS Receiver Specifications

- Acquisition time: <4 minutes from a cold start
- Re-acquisition time: <2 sec (90%)
- Frequency:
  - GPS L1 (1575.42 MHz)
  - GLONASS L1 (1602 MHz)
- Satellites tracked: up to 32 simultaneously
- Sync to UTC: within ±15 ns to GPS/UTC (1 sigma) (stationary)
- Accuracy horizontal position: <6 meters (50%) <9 meters (90%)
- Accuracy altitude position: <11 meters (50%) <18 meters (90%)

3.14 Temperature Sensor

The unit is equipped with an on-board temperature sensor.

- Operating temperature range: -40°C to 85°C (-40°F to 185°F)
- Accuracy: ±3°C max.
- Update rate: Once per second

3.15 Environmental Specifications

- Temperature:
  - Operating: -40°C to 75°C (-40°F to 167°F)
  - Storage: -40°C to 85°C (-40°F to 185°F)
- Humidity: Operating and storage: 5% to 95% RH, non-condensing
- Altitude: Operating: Up to 10,000 feet
- Storage: Supports commercial shipping altitudes

CHAPTER 4

Pinouts

This chapter discusses the following:

4.1 Pinouts 18
4.1.1 Timing Connector Pinout 18

4.1 Pinouts

The pinouts for the TSync-PCI-104 board are as follows:

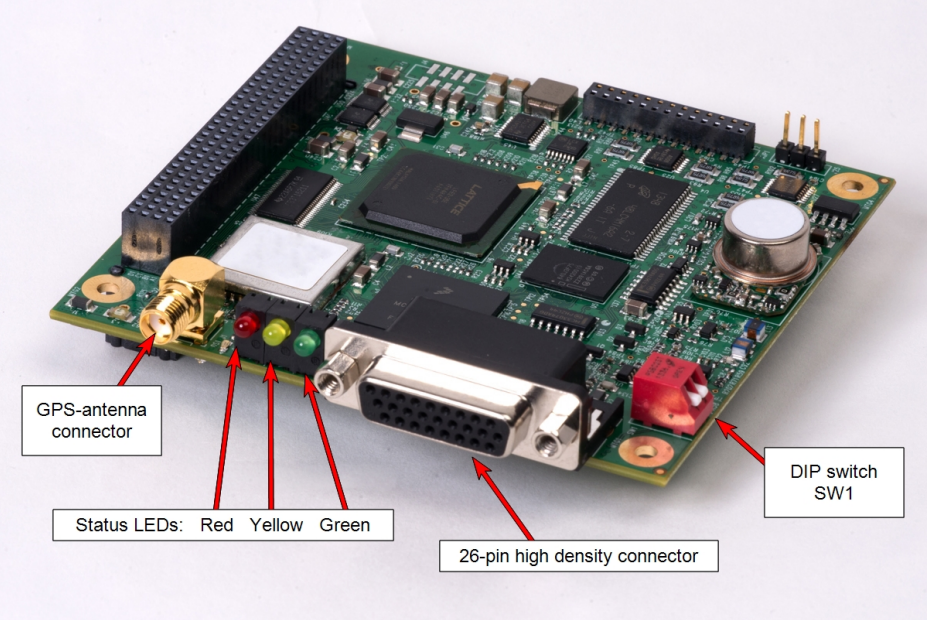


Figure 4-1: TSync-PCI-104 board

The timing interface connector supports all of the input and output references, and GPIO. It consists of a 26-pin high-density D-sub plug.

4.1.1 Timing Connector Pinout

Pin	Signal	Pin	Signal
1	GPIO Output 2	14	GPIO Output 3
2	Ground	15	Ground
3	GPIO Output 0	16	GPIO Output 1
4	GPIO Input 2	17	GPIO Input 3
5	Ground	18	Ground
6	GPIO Input 0	19	GPIO Input 1
7	External 1PPS Input	20	1PPS Output
8	Ground	21	Ground

Pin	Signal	Pin	Signal
9	IRIG AM Output	22	10MHz Output
10	IRIG AM Input +	23	Ground
11	IRIG AM Input -	24	IRIG DCLS Input -
12	IRIG DCLS Output -	25	IRIG DCLS Input +
13	IRIG DCLS Output +	26	Ground

Table 4-1: Timing Connector Pinout

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CHAPTER 5

Installation

This chapter discusses the following:

5.1 Card Configuration 22
5.2 GNSS Antenna 23
5.3 Card Installation 23
5.4 Status LEDs 24

Caution – Observe all ESD procedures when handling the board and the computer. Before installing the board, discharge static buildup by touching the metal frame of the computer with one hand and the protective bag containing the board with the other hand. Open the protective bag only after static buildup has been safely discharged.

5.1 Card Configuration

The max configuration for the PCI bus of PCI-104 modules is FOUR plus the host board. When stacking more than ONE PCI-104 module to a host board, the modules need to be set to different PCI numbers, using the DIP switch SW1.

Follow the installation procedure outlined under "Card Installation" on the facing page.

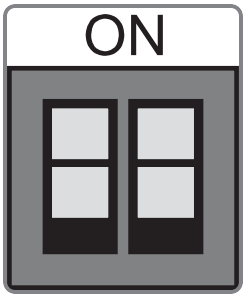


Figure 5-1: DIP-switch layout

Switch 1	Switch 2	Module Slot	INT # selected
OFF (*)	OFF (*)	1	INT A#/CLK 0/IDSEL 0
OFF	ON	2	INT B#/CLK 1/IDSEL 1
ON	OFF	3	INT C#/CLK 2/IDSEL 2
ON	ON	4	INT D#/CLK 3/IDSEL 3

Table 5-1: SW1 Settings [(*) = default]

5.2 GNSS Antenna

The mounting location of the external GNSS antenna should be free of objects that could obstruct satellite visibility from straight overhead to within 20 degrees of the horizon in all directions.

Obstructions that block a significant portion of the sky result in degraded performance. The GNSS receiver must track at least four satellites, in order to obtain time synchronization.

To optimize timing accuracy, the GNSS receiver attempts to track satellites that are spread out as far as possible across the sky. The GNSS antenna must be mounted such that the antenna points to the sky (i.e. the connector side pointing down), and it must be spaced at least 39 inches (1 meter) away from other GNSS antennas.

Mount the antenna at the desired location. Connect the supplied cable to the antenna. Take appropriate lightning precautions as necessary.

NOTE – Spectracom recommends applying an appropriate silicon grease to the cable connection at the GNSS antenna in order to protect the connection from moisture. An additional weatherproofing kit (P/N 221213) containing butyl rubber and plastic tape is also available from Andrews Corporation, US 800.255.1479.

5.3 Card Installation

Installation procedure

1. Always work at an ESD protected workstation, wearing a grounded wrist-strap.
2. Turn off power to the PCI-104 system.
3. Select the stand-offs for the desired stack height, and install them.
4. Remove the board from its anti-static bag.
5. Check that the pins of the bus connector are properly positioned.
6. Verify the stacking order. Make sure all of the busses used by the peripheral cards are connected to the CPU-module.
7. Hold the board by its edges and orient it such that the bus connector pins line up with the matching connector on the stack.
8. Carefully and evenly press the board onto the PCI-104 stack.
9. If other boards are to be stacked on top of this unit, install them.
10. Attach any necessary cables..

11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working correctly.

The board operates automatically as soon as the host computer system performs the power-on reset. To change the operating parameters or read data, consult the avail able Application Programmer's Guide for this product.

5.4 Status LEDs

During start up and operation, the board LEDs flash in sequence to indicate dif ferent operational states. The patterns are as follows:

State	Sync	Alarm	Holdover	1PPS	Manual
Power-On	On	Off	Off	N/A	N/A
Self-Test	On	On	On	N/A	N/A
Waiting for Host	Blink	Blink	Off	N/A	N/A
Download from Host	Strobe	Strobe	Strobe	N/A	N/A
Initialize	Off	Off	Off	-	Off
Never Synchronized	Off	Off	Off	-	N/A
Synchronized	On	Off	Off	-	N/A
Holdover	On	Off	On	-	N/A
No Longer Synchronized	Off	On	Off	-	N/A
Free Run	Blink	Off	Blink	-	N/A
• Fault	Code	Code	Code	Code	Code

Table 5-2: LED Flash Patterns

• The code indicates the fault condition. It blinks the number of times indicated with a 2-second pause between each set.
1 blink = FPGA programming error
2 blinks = failure to decompress
3 blinks = CRC failure writing to flash
4 blinks = self-test failure
5 blinks = timing system failure



NOTE – During the power-on, self-test, wait-for-host, and download-from-host states, modes are directly allocated to the LEDs (sync is green, holdover is yellow, and alarm is red). During normal operation, the user may set any LED to any of the operational modes.

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CHAPTER 6

Theory of Operation

The board's architecture essentially consists of input references, which are used as sources of 1PPS synchronization and/or time-of-day (TOD) and date information, and for disciplining an internal oscillator. The TSync-PCI-104 takes the synchronous clock, a 1PPS and time-of-day (TOD) and date to create output references that act as time references for other devices. Other interfaces for time stamping external events, cre ating precisely timed external signals, debug, upgrade, and access from a host computer are provided.

This chapter discusses the following:

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6.1 Input References

The input references consist of multiple interfaces to various types of Time References. A Time Reference can take many forms but their fundamental responsibility is they always provide a 1PPS on-time-point, they usually provide a time-of-day and date input and they might provide a control and status protocol to the time source. The input references can also provide other time related data such as Leap Second indication and number of seconds, Julian date, day of year, day of week, week of year, status, sync indication, accuracy indication and other fields unrelated to time.

The TSync-PCI-104 architecture's input reference subsystem is designed to support multiple possible input references, allowing only a single time reference and 1PPS reference to discipline the local clock subsystem. The user can choose to use the factory default priority list for input references, or may define a proprietary priority list. This user priority list can be created to combine different time and 1PPS sources (such as GNSS time coupled with the external 1PPS). The user is also provided with the means to enable or disable the selection of a specified input reference allowing them to disregard the list and synchronize to a specific output.

6.1.1 GNSS Receivers as Input References

GNSS receivers are usually the highest precision and accuracy time references a TSync-PCI-104 board can select. GNSS receivers use coaxial GNSS antenna input and typically provides a serial interface and a 1PPS output. The serial interface can be used for bi-directional communication with the GNSS receiver to implement a control and status protocol which conveys time and position information.

6.1.2 IRIG Inputs

Inter-range instrumentation group time codes, more commonly referred to as "IRIG" time codes, were created by the Tele-Communications Working Group of the Inter-Range Instrumentation Group, which is a standard body formed by Range Commanders Council. This standard was used by US Government military test ranges, NASA, and other research organizations to distribute telemetry information, including time and frequency. The current standard version is IRIG Standard 200-4. The TSync-PCI-104 architecture uses IRIG formats as both input and output references. IRIG formats can be amplitude modulated, or they can be digital signals at various carrier and clock rates.

The TSync-PCI-104 architecture supports IRIG inputs with Formats A, B, and G. It supports inputs and outputs using modulation frequency values of pulse width code, also known as DCLS (0), and sine wave amplitude modulated coding. Additionally, the board supports inputs with frequency/resolution values of no

carrier/index count interval, 1 kHz/1 ms, 10 kHz/0.1 ms, and 100 kHz/10 ms, as well as IRIG input coded expressions of the fields BCDTOY, CF, SBS, and BCDYEAR.

The TSync-PCI-104 board supports IRIG inputs of the following coded expressions combinations for BCDTOY, CF, SBS, and BCDYEAR fields:

- 0 – BCDTOY, CF, SBS
- 1 – BCDTOY, CF
- 2 – BCDTOY
- 3 – BCDTOY, SBS
- 4 – BCDTOY, BCDYEAR, CF, SBS
- 5 – BCDTOY, BCDYEAR, CF

The TSync-PCI-104 board supports synchronization with the following analog and DCLS IRIG input formats:

A – DCLS	A – AM	B – DCLS	B – AM	G – DCLS	G – AM
A – DCLS	A – AM	B – DCLS	B – AM	G – DCLS	G – AM
A000	A130	B000	B120	NA	NA
A001	A131	B001	B121	G001	G141
A002	A132	B002	B122	G002	G142
A003	A133	B003	B123	NA	NA
A004	A134	B004	B124	NA	NA
NA	NA	NA	NA	G005	G145

Table 6-1: IRIG Input Reference Formats

The TSync-PCI-104 supports the IRIG B variant NASA36 as an input format, as well as the IEEE C37.118-2005 (which is an IRIG B format with extensions as an input format). The IEEE C37.118-2005 specification supersedes IEEE 1344-1996. The TSync-PCI-104 is backward compatible to IEEE 1344-1996 by compliance with IEEE C37.118-2005.

The board can detect, automatically, IRIG formats A, B, G, and NASA36. IRIG format IEEE1344, coded expression, and control field information *cannot* be auto-detected, however. These must be specified by the user if these inputs are to be used.

NOTE – Always configure IRIG parameters in the following order: format, coded expressions, control field definitions.

In operation, the TSync-PCI-104 board receives IRIG input data and any time code messages transmitted, performs signal conditioning on the data, and decodes the data per its manually set parameters and automatically detected functions. In turn, the board provides a serial time code data message and a 1PPS reference. It also returns the IRIG input message's raw serial time code data in Spectracom's data format. (This is useful in debugging serial time code source and hardware implementations.)

The TSync-PCI-104 module also accepts as input any non-standard IRIG format generated by the Spectracom Netclock, including the non-standard BCDYEAR found in the Control field. This is intended to support the Spectracom 91xx and 92xx IRIG formats, which use the BCDYEAR in the Control field.

6.1.3 External 1PPS Reference

The board's external 1PPS reference provides the on-time-point for the current second. This reference is used by the TSync-PCI-104 as the primary source of frequency synchronization (while another input reference is required to serve as the source of time and date information). The external 1PPS reference can be set to use either the rising or falling edge.

6.1.4 Built-in References

The TSync-PCI-104 board provides built-in references that support specialized user applications.

6.1.4.1 Host Reference

The TSync-PCI-104 can be set to use the host as the source of date and time information, while another input reference is required to serve as the source of frequency input. This allows the host to provide time to the board while providing a means to determine and indicate whether that time is valid for synchronization. Using the host as a reference means it could conceivably be used to receive date and time information from a source not available to the board, providing that information to the board for synchronization to it (while using a separate frequency input).

6.1.4.2 Self Reference

The TSync-PCI-104 provides a built-in reference that allows the board to operate without a separate input reference. The date and time or frequency information from this self reference is always considered valid. This allows a user to operate the board as if it were synchronizing to an input reference, without a valid external ref erence input. The self reference priority table entry defaults to "disabled."

6.2 Input Reference Monitor

The input reference monitor subsystem maintains the reference priority table and determines which input reference(s) are selected to synchronize the clock sub system.

Three tables are maintained by the system:

- A default table, which provides the default reference pairings in timing accuracy priority
- A working table, which is the table used for selecting reference inputs
- A user table, which can be stored persistently and, if present, will be loaded into the working table at startup

Enable	Priority	Time Ref	1PPS Ref
en	1	gps0	gps0
en	2	ird0	ird0
en	3	ira0	ira0
en	4	hst0	epp0
en	5	hst0	self
dis	6	self	self
dis	0		
dis	0		

gps = GPS Reference, ird = IRIG DCLS Reference, ira = IRIG AM Reference, epp = External 1PPS Reference, hst0 = Host Reference, self = Self Reference

Table 6-2: Example Default Table

Entries can be added to and deleted from the working table. In addition, individual entries can be enabled or disabled. Their priorities can be changed at any time.

Any changes to the table will cause the reference monitor to reevaluate the best ref erence to use for synchronization. The working table can be saved to the user table and persisted, or it can be reset to the default table or an already existing user table at any time.

At any given time, the highest priority enabled entry in the table that has both a valid time and a valid 1PPS reference will be used as the best reference for syn chronization. The power of the reference monitor is in its ability to generate any com bination of time and 1PPS references in any priority. For example, if a user has a high precision 1PPS source, this can serve as the provided external 1PPS reference and can be paired with a GPS time reference.

The reference tables, the currently selected best reference, and the current validity states of all input references can be requested from the board.

6.3 Clock Subsystem

The clock subsystem is the heart of the TSync-PCI-104 timing architecture. Time is maintained in the board's hardware and incremented in 5 nsec units, while sub-second information is tracked. Time, from seconds through years, is incremented based on the internal 1PPS derived from the selected input reference.

By default, system time is maintained in UTC, but this can be set to TAI, GPS, or a local timescale (with DST rules). Offsets between timescales are maintained on the board to facilitate conversions between the timescales. The offsets can be set by the user or, depending on the references available, may be automatically determined. Users who wish to use a specific timescale must provide the timescale offset from an input reference or by setting it manually.

The clock subsystem can handle several types of time discontinuities, including leap years, leap seconds, DST transitions, and a user-settable discontinuity. Leap years are automatically detected and handled by the system. Leap seconds, if set from the user or received from an input reference, are also handled accordingly. The sys tem can manage DST transitions set by the user when running in a local timescale.

6.4 Output References

The output subsystem provides time code and frequency references derived from the input reference. The outputs provided include a single IRIG AM and DCLS out put pair, a 10-MHz sine wave output, and a 1PPS output.

The output subsystem supports setting output offset(s) for each output except the 10-MHz sine wave output, which can be used to compensate for output cable length

delays or downstream clock accuracy errors. Each output offset can range from -500 msec to +500 msec in 5 or 20 nsec steps (depending on the output).

6.4.1 IRIG Output

The TSync-PCI-104 board provides one IRIG AM and DCLS pair output. The IRIG output is a rolling count of the initial value of the system time until synchronized. The board drives the IRIG AM output from an associated IRIG DCLS output and outputs the exact same format (except for the AM modulation).

The TSync-PCI-104 board supports IRIG outputs with Formats A, B, E and G. It also supports IRIG outputs using modulation frequency values of pulse width code, also known as DCLS, and sine wave amplitude modulated coding. It further supports IRIG outputs with frequency/resolution values of no carrier/index count interval, 100 Hz/10 ms, 1 kHz/1 ms, 10 kHz/0.1 ms, and 100 kHz/10 ms. Coded expressions for the fields BCDTOY, CF, SBS, and BCDYEAR. Are supported, as is IRIG output for the following coded expressions combinations for BCDTOY, CF, SBS, and BCDYEAR fields:

- 0 – BCDTOY, CF, SBS
- 1 – BCDTOY, CF
- 2 – BCDTOY
- 3 – BCDTOY, SBS
- 4 – BCDTOY, BCDYEAR, CF, SBS
- 5 – BCDTOY, BCDYEAR, CF

The TSync-PCI-104 board allows the user to select the following Time Code Formats for IRIG output:

A – DCLS	A – AM	B – DCLS	B – AM	E – DCLS	E – AM	G – DCLS	G – AM
A000	A130	B000	B120	E000	E110	NA	NA
A001	A131	B001	B121	E001	E111	G001	G141
A002	A132	B002	B122	E002	E112	G002	G142
A003	A133	B003	B123	E003	E120	NA	NA
A004	A134	B004	B124	E004	E122	NA	NA
NA	NA	NA	NA	E005	E125	NA	G145

Table 6-3: IRIG Output Reference Formats

The TSync-PCI-104 allows the user to select the IRIG B variant NASA36 as an IRIG output. It also supports user-selection of IEEE C37.118-2005 as an IRIG output. This is an IRIG B format with extensions. The TSync-PCI-104 board is compliant with IEEE 1344-1996 as IEEE C37.118-2005 supersedes this specification.

The board generates the non-standard IRIG formats that are generated by the Spec tracom Netclock, including the non-standard BCDYEAR. This provides for com patibility with existing Spectracom NetClock products.

NOTE – Configuration of IRIG parameters should always be in the following order: format, coded expressions, control field definitions.

The TSync-PCI-104 board supports adjustment of the IRIG output amplitude using a scale ranging from 0 to 255, with 128 being the middle and default value. The adjustment range approximates a linear function.

The IRIG outputs provide an offset that can be applied to adjust its relationship with the internal system 1PPS, from -500 msec to +500 msec in 5 nsec increments

The IRIG outputs provide signature control, which enables and disables outputs under the following conditions:

- Signature control off — outputs always on.
- Signature control enables output when in sync to input reference only
- Signature control enables output when in sync to input reference or in hol dover

6.4.2 10-MHz Sine Wave Output

The TSync-PCI-104 board generates a 10-MHz sine wave output from the dis ciplined on-board oscillator. The 10-MHz sine wave output provides signature con trol similar to the IRIG outputs.

6.4.3 1PPS Output

The TSync-PCI-104 board generates a digital 1PPS output from the internal 1PPS of the system. Several parameters of the 1PPS can be controlled. The active edge can be set to either rising or falling edge, the pulse width can be adjusted, and an offset can be applied to adjust its relationship to the internal system, 1PPS from -500 msec to +500 msec in 5-nsec increments. The 1PPS output provides signature control similar to the IRIG outputs.

6.5 General Purpose Input/Output

The TSync-PCI-104 board has four general purpose input (GPIO) pins and four general purpose output (GPIO) pins. The General I/O subsystem provides a mechanism to generate or time stamp external events, to match times and generate a signal, to create Heartbeat pulses, or to create square wave clock signals synchronous to the internal timing system clock and to the 1PPS signal from the input reference.

6.5.1 Programmable Inputs

The General I/O input pins support user selection for detection of rising edge or falling edge input events. These inputs, when triggered, are used to time-tag the input edge-detected events. They support a time between input events of 50 nsec and an overall rate of more than 10,000 time stamps per second. Time stamps are maintained in a FIFO on the board that can store up to 512 unique time stamps among all input pins.

6.5.2 Programmable Outputs

The user may select the operational mode of the General I/O outputs pins, setting them to generic output pins, square wave generation, and match time events.

The General I/O outputs, when configured as generic output pins, can be controlled and changed at the user's discretion.

The General I/O output can be programmed as a square wave synchronized to the 1PPS. When used to output a square wave, the General I/O has a programmable period range of 100 nsec to 1 sec (10 MHz to 1 Hz) in 5 nsec steps and a programmable pulse width of 10 nsec to 999,999,990 nsec in 5 nsec steps (polarity is programmable).

The General I/O is configurable as a Match Time Event pin, which will activate at a preset time and become inactive at another preset time. The Match Time Event provides two user settable times to make the General I/O pin active and inactive. The Match Time Event configured General I/O pin has a programmable edge, allowing the selection of Low to High or High to Low.

The General I/O output signals timing are accurate relative to the Input reference's 1PPS signal to within ±50 nsec. The General I/O output has a programmable offset, which ranges from -500 msec to +500 msec in 5 nsec steps.

6.6 System Status

The TSync-PCI-104 board maintains status information. It logs error and informational messages while operational. System status information (synchronization status, holdover status, freerun status, and total system uptime) are available to the user. In addition, alarm conditions and time stamps for the alarms are available for conditions including synchronization, holdover, frequency errors, PPS specification errors, reference changes, and system errors.

6.7 LEDs

The TSync-PCI-104 board includes three LEDs that provide visual status information to the user. Refer to the table "LED Flash Patterns" on page 24 for these indicator codes. The LEDs operate in certain modes by default, but each LED can be configured independently to display any mode, including a manual mode. In manual mode, the user can set LEDs to on, off, or blink.

6.8 Upgrade

One of the most powerful features available is the capability to perform field upgrades of the configuration and firmware/FPGA loads for the TSync-PCI-104 boards. New features and capabilities can be added and uploaded to the board without the need to restart the system in which the board is installed. Refer to the Factory Driver Guide for details on upgrading the board using the upgrade tool supplied with the driver.

6.9 Interrupts

The host bus has one interrupt line available from the TSync-PCI-104 . All interrupt sources destined for the host bus are multiplexed on the single interrupt line. All interrupts are masked on startup, but can be unmasked using the host bus interrupt mask register. Whether an interrupt is masked or not, the current state of the interrupt is available by reading the Host Bus Interrupt Status register. All interrupt sources are latched based on an edge transition. All interrupts are cleared in the host bus interrupt status register.

6.9.1 Interrupt Descriptions

6.9.1.1 1PPS Received

This interrupt is driven on the incident edge of the PPS.

6.9.1.2 Timing System Service Request

This interrupt is used by the micro to request attention from the local bus.

6.9.1.3 Local/µC Bus FIFO Empty

This interrupt is driven when the FIFO from the local bus to the microcontroller bus becomes empty. It is based on the rising edge of the FIFO's empty flag.

6.9.1.4 Local / µC Bus FIFO Overflow

This interrupt is driven when the FIFO from the local bus to the microcontroller bus is overflowed. It is based on the rising edge of the FIFO's overflow flag.

6.9.1.5 µC / local bus FIFO Data Available

This interrupt is driven when the FIFO from the microcontroller bus to the local bus is no longer empty. It is based on the falling edge of the FIFO's empty flag.

6.9.1.6 µC / local bus FIFO Overflow

This interrupt is driven when the FIFO from the microcontroller bus to the local bus is overflowed. It is based on the rising edge of the FIFO's overflow flag.

6.9.1.7 GPIO Input x Event

This interrupt is driven when the active edge of the GPIO input signal is received.

6.9.1.8 GPIO Output x Event

The interrupt is driven when an event occurs in the GPIO output. An event depends on the mode of operation of the GPIO output. In Direct mode, an event is triggered when the output Value in the GPIO output control / status register is changed and creates the active edge selected by the GPIO direct mode output interrupt active edge bit in that same register. This can be used to generate a “software” interrupt by setting the GPIO output appropriately. In match time mode, an interrupt is gen erated whenever the GPIO output high match time or GPIO output low match time registers are enabled and subsequently matched against the current system time. In square wave mode, an interrupt is generated whenever the GPIO output generates the active edge as selected by the GPIO output square wave active edge bit in the GPIO output control / status register. This can be used to generate a periodic inter rupt at the rate of the square wave.

6.9.1.9 Time Stamp Data Available

This interrupt is driven when the time stamp FIFO goes non-empty. Time stamp data is available in the time stamp FIFO when this interrupt occurs.

CHAPTER 7

Options and Accessories

This chapter discusses the following:

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7.2.2 Basic Breakout Cable 42
7.2.3 GNSS Cables 44

7.1 Options

A TCXO oscillator is standard. An available OCXO oscillator may be purchased as an option.

7.2 Accessories

7.2.1 Premium Breakout Cable

The premium breakout cable breaks out all features from the 26-pin timing con nector to separate BNC and DB-9 connectors for use. See table below for details.

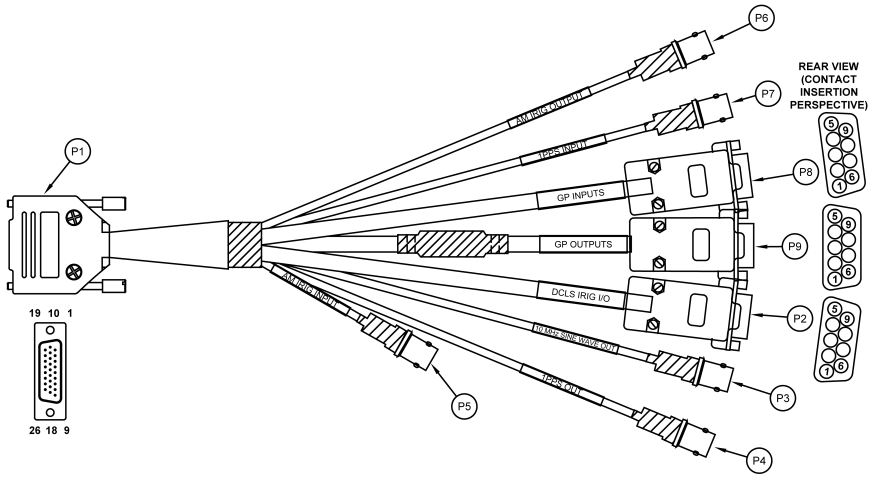


Figure 7-1: Breakout cable, premium version

Pin	Signal	Pin	Signal
P1—TIMING CONNECTOR			
1	GPIO Output 2	14	GPIO Output 3
2	Ground	15	Ground
3	GPIO Output 0	16	GPIO Output 1
4	GPIO Input 2	17	GPIO Input 3
5	Ground	18	Ground

Pin	Signal	Pin	Signal
6	GPIO Input 0	19	GPIO Input 1
7	External 1PPS Input	20	1PPS Output
8	Ground	21	Ground
9	IRIG AM Output	22	10MHz Output
10	IRIG AM Input +	23	Ground
11	IRIG AM Input -	24	IRIG DCLS Input -
12	IRIG DCLS Output -	25	IRIG DCLS Input +
13	IRIG DCLS Output +	26	Shield
P2—IRIG DCLS I/O (DB-9 FEMALE)			
2	Ground	6	IRIG DCLS Output +
3	Ground	7	IRIG DCLS Output -
4	IRIG DCLS Input +	BS	Ground
5	IRIG DCLS Input -		
P3—10MHZ OUTPUT (BNC FEMALE)			
1	10MHz Output	BS	Ground
P4—1PPS OUTPUT (BNC FEMALE)			
1	1PPS Output	BS	Ground
P5—IRIG AM INPUT (BNC FEMALE)			
1	IRIG AM Input +	BS	IRIG AM Input -
P6—IRIG AM OUTPUT (BNC FEMALE)			
1	IRIG AM Output	BS	Ground
P7—1PPS INPUT (BNC FEMALE)			
1	External 1PPS Input	BS	Ground
P8—GP INPUT (DB-9 FEMALE)			
1	GPIO Input 0	7	Ground
2	GPIO Input 1	8	Ground
3	GPIO Input 2	9	Ground

Pin	Signal	Pin	Signal
4	GPIO Input 3	BS	Ground
6	Ground		
P9—GP OUTPUT (DB-9 FEMALE)			
1	GPIO Output 0	7	Ground
2	GPIO Output 1	8	Ground
3	GPIO Output 2	9	Ground
4	GPIO Output 3		
6	Ground	BS	Ground

Table 7-1: Pinout, premium breakout cable (unspecified pins are not connected in the cable)

7.2.2 Basic Breakout Cable

The basic breakout cable breaks out a subset of features from the 26-pin timing con nector to separate BNC and DB-9 connectors for use. The basic breakout cable sup ports the following features: External 1PPS Input, IRIG AM Input, IRIG DCLS Input, IRIG AM Output, (1) GP Input, (2) GP Outputs. The pinout of the connector is depic ted below:

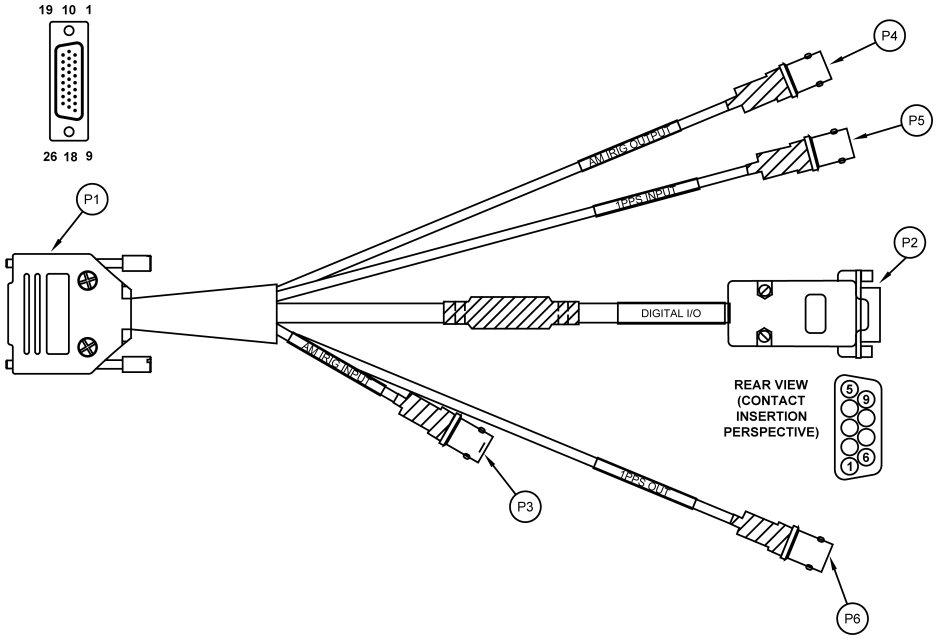


Figure 7-2: Breakout cable, basic version

Pin	Signal	Pin	Signal
P1—TIMING CONNECTOR		P2—DIGITAL I/O (DB-9 FEMALE)	
3	GPIO Output 0	11	IRIG AM Input -
5	Ground	16	GPIO Output 1
6	GPIO Input 0	18	Ground
7	External 1PPS Input	21	Ground
8	Ground	24	IRIG DCLS Input -
9	IRIG AM Output	25	IRIG DCLS Input +
10	IRIG AM Input +		
P2—DIGITAL I/O (DB-9 FEMALE)			
1	Ground	6	GPIO Output 0
2	GPIO Input 0	7	Ground
3	Ground	8	GPIO Output 1
4	IRIG DCLS Input +	9	Ground

Pin	Signal	Pin	Signal
5	IRIG DCLS Input -	BS	Ground
P3 — IRIG AM INPUT (BNC FEMALE)			
1	IRIG AM Input +	BS	IRIG AM Input -
P4 — IRIG AM OUTPUT (BNC FEMALE)			
1	IRIG AM Output	BS	Ground
P5 — 1PPS INPUT (BNC FEMALE)			
1	External 1PPS Input	BS	Ground
P6 — 1PPS OUTPUT (BNC FEMALE)			
1	1PPS Output	BS	Ground

Table 7-2: Pinout, basic breakout cable (unspecified poins are not connected in the table)

7.2.3 GNSS Cables

Contact Spectracom for more information on GNSS cable length options.

CHAPTER 8

Driver Support

Spectracom offers an Application Programmer's Guide for the TSync-PCI-104 , as well as specific drivers and supporting documentation.

Please contact your sales representative for more information about Spectracom's bus-level timing board driver support for a variety of operating platforms. You may also visit our website at www.spectracomcorp.com to download datasheets and manuals.

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APPENDIX

Appendix

This appendix comprises lists of figures and tables, and information about the revision version of this User Manual.

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Document Revision History

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A	3449	User Manual for new product, first iteration	May 5, 2014

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